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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,699	05/21/1999	WILLIAM J. DALLY	AVI99-01	8189

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EXAMINER
LY, ANH VU H

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 05/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/316,699	DALLY ET AL.	
	Examiner	Art Unit	
	Anh-Vu H Ly	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-45 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-7, 11-14, 16-22, 26-29, 31-35, 38, and 40-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong et al. (US Patent No. 6,311,212). Hereinafter, referred to as Chong.

With respect to claims 1 and 31, Chong discloses in Figure 2, a fast access memory, Rx cache 165 and Tx cache 175 (a first set of rapidly accessible buffers for the information units).

Further, Chong discloses in Figure 2, a local memory 115 (a second set of buffers for the information units that are accessed more slowly than the first set).

Furthermore, Chong discloses (col. 5, lines 25-27) that VCDs stored in the Rx cache 165 are retrieved and processed much quicker than those VCDs stored only in local memory 115.

With respect to claims 2, 17, and 32, Chong discloses (col. 3, lines 37-41) that all components of processing engine 10 reside on a single chip but all components may be spread across many chips such that processing engine 10 is implemented using many chips (the router is implemented on one or more integrated circuit chips).

Chong discloses in Figure 2, that fast access memory, Rx cache 165 and Tx cache 175, is on-chip memory (first set of buffers are located on the router integrated circuit chips). And local memory 115 is off-chip memory (second set of buffers are located on memory chips separate from the router integrated circuit chips).

With respect to claims 3, 18, 33, and 41, Chong discloses (col. 4, lines 55-66) that upon receiving a cell for a VC that has been registered, receiver engine 160 determines the VCD address using an information field from the cell header, such as VCI/VPI field. After the VC-ID has been determined, the VCD is fetched by receiver engine 160 and stored in Rx cache 165.

Chong discloses (col. 4, lines 32-34) that for applications requiring more than 128 VCs, local memory 115 is required to store additional VC descriptors. This means, local memory 115 is used to store additional VC descriptors when the internal memory exceeded its capacity and it contains all the necessary information for VCs (second set of buffers holds information units for a complete set of virtual channels).

With respect to claims 4, 19, 34, and 42, Chong discloses (col. 5, lines 28-33 and Figure 3) that CAM190 (pointer array) includes a list of VC-IDs associated with the VCDs that have been stored to Rx cache 165 (a buffer pool). Associated with each VC-ID is the address in Rx cache 165 where the associated VCD is stored.

With respect to claims 5, 20, 35, and 43, Chong discloses in Figure 2, a fast access memory, Rx cache 165 and Tx cache 175 (first set buffers is organized as a set-associative cache).

With respect to claims 6 and 21, Chong discloses (col. 5, lines 28-33 and Figure 3) that CAM190 includes a list of VC-IDs associated with the VCDs that have been stored to Rx cache 165. Associated with each VC-ID is the address in Rx cache 165 where the associated VCD is stored (each entry in the set associative cache contains a single information unit).

With respect to claims 7 and 22, Chong discloses (col. 4, lines 55-66) that upon receiving a cell for a VC that has been registered, receiver engine 160 determines the VCD address using an information field from the cell header, such as VCI/VPI field. After the VC-ID has been determined, the VCD is fetched by receiver engine 160 and stored in Rx cache 165 (each entry in the set associative cache contains the buffers and state for an entire virtual channel).

With respect to claims 11, 12, 26, and 27, the limitations, miss status registers to hold information units waiting for access to the second set of buffers and eviction buffer to hold entries staged for transfer from the first set of buffers to the second set of buffers, are inherently disclosed by Chong.

Chong discloses (col. 4, lines 30-36) that the internal memory 80 is of sufficient size to store up to 128 VC descriptors. For applications requiring more than 128 VCs, local memory 115 is required to store additional VC descriptors. Further, Chong discloses (col. 3, lines 50-55) that local memory interface block 15 provides a connection to a local off-chip system memory such as DRAM, SRAM, SDRAM, SSRAM or any combination thereof. DMAC 25 provides control of data transfers between external memories, internal memory 80 and the local memory. This means, VC descriptors must be queued and lined up in a memory or a buffer for transferring to the local memory115 when the internal memory exceeded its capacity.

With respect to claims 13 and 28, Chong discloses (col. 3, lines 31-37) that the network processing engine is useful for a variety of network communications applications including implementation in multi-protocol network NICs, server NICs, workgroup, IP and ATM switches, multi-protocol and IP routers, ATM backbone switch applications multi-protocol/ATM adapters and the like (router is in a multi-computer interconnection network).

With respect to claims 14, 29, and 38, Chong discloses (col. 3, lines 31-37) that the network processing engine is useful for a variety of network communications applications including implementation in multi-protocol network NICs, server NICs, workgroup, IP and ATM switches, multi-protocol and IP routers, ATM backbone switch applications multi-protocol/ATM adapters and the like (fabric router is in a network switch or router).

With respect to claims 16 and 40, Chong discloses (col. 4, line 64 – col. 5, line 13) that VCDs are stored in Rx cache 165 because access time for Rx cache 165 is typically much shorter than for local memory 115 (storing information units in a first set of rapidly accessible buffers).

Chong discloses (col. 4, lines 32-34) that for applications requiring more than 128 VCs, local memory 115 is required to store additional VC descriptors (storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8, 10, 23, 25, 36-37, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Barkey et al. (US Patent No. 5,825,748). Hereinafter, referred to as Barkey.

With respect to claims 8, 23, 36-37, and 44, Chong discloses a system and a method for storing or caching, VC descriptors on a single-chip network processor, to enhance system performance.

Chong does not disclose a flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

Barkey discloses (see Abstract) a credit-based flow control scheme for controlling data communications (flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a flow control method in Chong's system, as disclosed by Barkey, for controlling data communications.

With respect to claims 10 and 25, as noted in the rejection statements of claim 8, Barkey discloses a credit-based flow control scheme for controlling data communications (flow control is credit-based).

3. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong and Barkey in view of Stephens et al. (US Patent No. 6,345,040). Hereinafter, referred to as Stephens.

With respect to claims 9 and 24, Chong discloses a system and a method for storing or caching, VC descriptors on a single-chip network processor, to enhance system performance.

Chong and Barkey do not disclose flow control is blocking.

Stephens discloses (col. 2, lines 41-50) that in a non-blocking input buffered switch with FIFO queuing, when the cell at the head of the queue is blocked due to contention for a given output port, all cells behind it within the queue are prevented from being transmitted. This situation is called head-of-line blocking (flow control is blocking).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adopt head-of-line blocking method in Chong's system, as disclosed by Stephens, for controlling data communications.

4. Claims 15, 30, 39, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Thorson et al. (US Patent No. 5,701,416). Hereinafter, referred to as Thorson.

With respect to claims 15, 30, 39, and 45, Chong discloses a system and a method for storing or caching, VC descriptors on a single-chip network processor, to enhance system performance.

Chong discloses (col. 3, lines 31-37) that the network processing engine is useful for a variety of network communications applications including implementation in multi-protocol network NICs, server NICs, workgroup, IP and ATM switches, multi-protocol and IP routers (fabric router), ATM backbone switch applications multi-protocol/ATM adapters and the like.

Chong does not disclose information units are flits.

Thorson discloses (col. 1, lines 60-62) that the packet is divided into a number of smaller message packets called flow control units (flits).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a method of dividing a packet into a number of smaller message packets (flits) in Chong's system, as disclosed by Thorson, to utilize in a store and forward type network where packets are transferred as single units from node to node along the path from the source to destination.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Simmons et al. (US Patent No. 6,084,856) discloses a method and apparatus for adjusting overflow buffers and flow control watermark levels.

Shigeeda (US Patent No. 5,737,748) discloses a microprocessor unit having a first level write-through cache memory and a smaller second level write-back cache memory.

Runaldue et al. (US Patent No. 6,233,244) discloses a method and apparatus for reclaiming buffers.

Melchior (US Patent No. 6,226,710) discloses a CAM engine.

Sekine et al. (US Patent No. 6,101,188) discloses an internetworking router.

Pierce et al. (US Patent No. 5,898,826) discloses a method and apparatus for deadlock-free routing around an unusable routing component in an N-Dimensional network.

Van Seters et al. (US Patent No. 5,812,775) discloses a method and apparatus for internetworking buffer management.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

avl
May 20, 2002

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